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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,993	04/21/2004	Harold Alexis Huggins	HUGGINS 7	5503

47396 7590 11/29/2005

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EXAMINER	
LIE, ANGELA M	

ART UNIT	PAPER NUMBER
2821	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,993	HUGGINS, HAROLD ALEXIS	
	Examiner	Art Unit	
	Angela M. Lie	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33 and 35* is/are rejected.

7)☒ Claim(s) *34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2,4-6, 8,10-15,17,18,20,22,29-31,33 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Krishaswamy et al (US Patent 5853601).

As to claim 1, Krishaswamy discloses a method for making a radio frequency (RF) component comprising: forming dielectric layer (Figure 5G, element 103) on a semiconductor substrate (Figure 5G, element 101); forming and patterning a conductive layer on the dielectric layer to define the RF component (Figure 5G, elements 105 and 109); forming at least one opening (Figure 5G, element 113) though the RF component (Figure 5G, elements 103, 105 and 109) at least to the semiconductor substrate (Figure 5G, element 101); and releasing the RF component from the semiconductor substrate (Figure 5G, element 117; column 2, lines 55-56) by exposing the semiconductor substrate to an etchant passing though the at least one opening to the semiconductor substrate.

As to claims 2 and 15, Krishaswamy discloses the method wherein releasing comprises exposing the semiconductor substrate to a dry etchant (column 2, lines 55-56).

As to claims 4 and 35, Krishaswamy discloses the method wherein forming the at least one opening (Figure 5D, element 113) comprises forming a plurality of openings (Figure 5D, first opening through element 111, and second opening through element 103) comprises forming a plurality of openings laterally adjacent portions of the conductive layer with no openings extending through the conductive layer (as shown in Figure 5D, elements 105 and 109 do not have any openings).

As to claims 5,17 and 30, Krishaswamy discloses the method wherein forming the plurality of openings comprises forming the plurality of openings (Figure 5D, element 113) comprises forming the plurality of openings in a predetermined pattern (before anything is manufactured, the outline has to predetermined, therefore those openings are considered to be in predetermined pattern).

As to claims 6,18 and 31, Krishaswamy discloses the method, wherein the predetermined pattern has substantially uniform spacing between adjacent openings (as shown in figure 5D).

As to claims 8 and 20, Krishaswamy discloses the method wherein the conductive layer comprises aluminum (column 2, lines 1-2).

As to claims 10 and 33, Krishaswamy discloses the method wherein forming the at least one opening comprises forming the at least one opening to have a diameter in a range of about .5 to 20 um (column 6, lines 44-46, since the thickness of dielectric (Figure 5D, element 103) is about 1 um, just by looking at the ratios or proportions of the elements in respect to each other, one can clearly see that diameter of the opening is approximately 2-3 microns).

As to claims 11 and 22, Krishaswamy discloses the method wherein the semiconductor substrate comprises silicon (column 6, line 51).

As to claim 12, Krishaswamy discloses the method wherein the at least one opening (Figure 5E, element 113) extends into the semiconductor substrate (Figure 5E, element 101).

As to claim 13, Krishaswamy discloses the method wherein the at least one opening (Figure 5D, element 113) substantially terminates at a surface of the semiconductor substrate (Figure 5D, element 101).

As to claim 14, Krishaswamy discloses a method for making a radio frequency (RF) component comprising: forming dielectric layer (Figure 5G, element 103) on a semiconductor substrate (Figure 5G, element 101); forming and patterning a conductive layer on the dielectric layer to define the RF component (Figure 5G, elements 105 and 109); forming a plurality of openings (Figure 5G, element 113) though the dielectric layer (Figure 5G, element 103) at least to the semiconductor substrate (Figure 5G, element 101); and releasing the RF component from the semiconductor substrate (Figure 5G, element 117; column 2, lines 55-56) by exposing the semiconductor substrate to an etchant passing though the openings to the semiconductor substrate.

As to claim 29, Krishaswany discloses a radio frequency (RF) component comprising: a dielectric layer (Figure 5F below, element 103) having opposing first and second major surfaces, the first surface being free from a semiconductor substrate (semiconductor is etched away, leaving air gap behind), the dielectric layer having a plurality of openings (Figure 5F below, element 113) extending between the first and

second opposing major surfaces; and a patterned conductive layer (Figure 5F below, elements 105 and 109) on the second major surface of the dielectric layer.

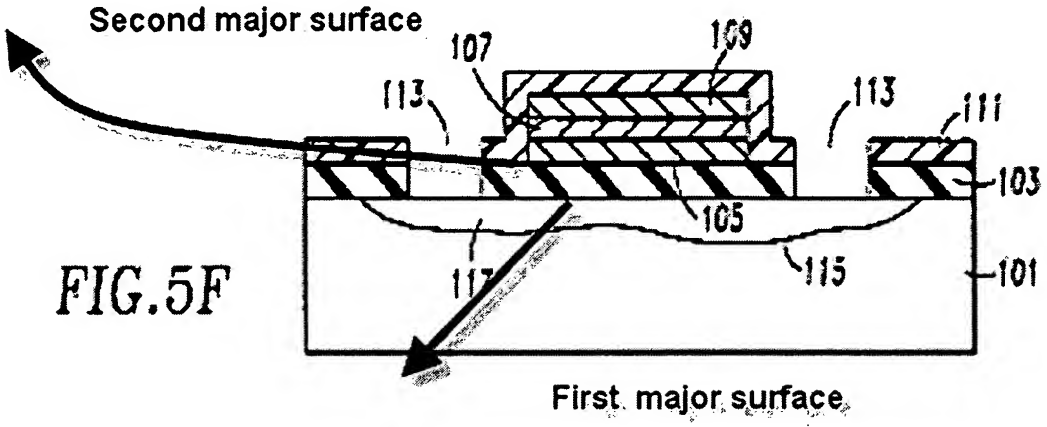

FIG.5F

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3,16,23,24,26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishaswamy et al (US Patent 5853601) in the view of Dr.Paul May (MSc Physics of Advanced Semiconductor Materials).

As to claims 3 and 16, Krishaswamy teaches the invention as disclosed in claim 2, however he does not teach that dry etchant comprises XeF2. Dr. May teaches dry etch comprising XeF2 (page 8, paragraph 1). It would have been obvious to one of the ordinary skill in the art during the time the invention was made to use dry etchant

comprising XeF2 as taught by Dr. May, because XeF2 in combination with Argon ions results in high anisotropy, good pattern definition, low damage and good selectivity to underlying (page 8, Adventages).

As to claim 23, Krishaswamy teaches a method for making a radio frequency (RF) component comprising: forming a dielectric layer (Figure 5E, element 103) on a semiconductor substrate (Figure 5E, element 101); forming and patterning a conductive layer (Figure 5E, elements 105 and 109) on the dielectric layer (103) to define the RF component; forming a plurality of openings (Figure 5E, element 113) trough the dielectric layer in a predetermined pattern at least to the semiconductor substrate (101); and releasing the RF component from the semiconductor substrate by exposing the semiconductor substrate to an etchant passing through the openings to the semiconductor substrate (Figure 5G, element 117; column 2, lines 55-56). Krishaswany does not disclose however, that etchant comprises XeF2. Dr. May teaches dry etch comprising XeF2 (page 8, paragraph 1). It would have been obvious to one of the ordinary skill in the art during the time the invention was made to use dry etchant comprising XeF2 as taught by Dr. May, because XeF2 in combination with Argon ions results in high anisotropy, good pattern definition, low damage and good selectivity to underlying (page 8, Adventages).

As to claim 24, Krishaswamy discloses the method, wherein the predetermined pattern has substantially uniform spacing between adjacent openings (as shown in figure 5D).

As to claim 26, Krishaswamy discloses the method wherein the conductive layer comprises aluminum (column 2, lines 1-2).

As to claim 28, Krishaswamy discloses the method wherein the semiconductor substrate comprises silicon (column 6, line 51).

5. Claims 7,19,25 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishaswamy et al (US Patent 5853601). Krishaswamy discloses the claimed invention except for substantially uniform spacing being in a range of about 20 to about 200 microns. It would have been an obvious matter of design choice to change the spacing length from 10 microns as taught by Krishaswamy (ratio relation from the drawings) to about 20 to 200 microns, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Furthermore the other important thing to note is the fact that the spacing between the openings does not change the functionality of the device. The only limiting factor in making the spacing very large, is the etching process, i.e. if spacing is too large it might be very hard to etch Silicon substrate completely under the dielectric layer.

6. Claims 9,21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishaswamy et al (US Patent 5853601) in the view of Sherrer et al (US Publication 2001/0050266). Krishaswamy teaches the method as disclosed in claims 1,14 and 23 respectively, he does not teach however that the dielectric layer comprises SiN. Sherrer teaches a dielectric surface used as a etch-stop layer comprising SiN. It would have been obvious to one of the ordinary skill in the art during the time the

invention was made to use a dielectric layer comprising SiN, because this dielectric is very well known in the art, and it performs the same function as SiO2, therefore they could be used interchangeably. This is definitely an advantage because if one of those dielectrics is cheaper than the other, by choosing cheaper material still performing same function, manufacturing cost could be cut down.

Allowable Subject Matter

7. Claim 34 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose the RF component as disclosed in claim 29, wherein each opening has respective rounded over edges adjacent the first and second major surfaces.

The Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US Patent 6093330 discloses a microfabrication process for enclosed microstructures comprising conductor, openings and substrate, wherein the etching is performed through the openings.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angela M. Lie whose telephone number is 571-272-8445. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Angela M Lie

WILSON LEE
PRIMARY EXAMINER